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Paper 11
Date: May 20, 2020

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

XMTT, INC.,
Patent Owner.

IPR2020-00145
Patent 7,707,388 B2

Before PHILLIP J. KAUFFMAN, MICHELLE N. WORMMEESTER, and BRENT M. DOUGAL, *Administrative Patent Judges.*

KAUFFMAN, *Administrative Patent Judge*.

DECISION
Instituting *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background

Intel Corporation ("Petitioner") filed a Petition (Paper 2, "Pet.") to institute an *inter partes* review of claims 1–39 (the "challenged claims") of U.S. Patent No. 7,707,388 B2 (Ex. 1001, "the '388 patent"). *See* 35 U.S.C. § 311. XMTT, Inc. ("Patent Owner") timely filed a Preliminary Response.

Paper 8 ("Prelim. Resp."). Applying the standard set forth in 35 U.S.C. § 314(a), we determine that Petitioner has demonstrated a reasonable likelihood of prevailing with respect to at least one of the challenged claims. Consequently, we institute, on behalf of the Director, an *inter partes* review of all challenged claims on all grounds. 37 C.F.R. § 42.4(a).

B. Related Matters

The parties identify as a related proceeding the co-pending district court litigation of *XMTT, Inc. v. Intel Corporation*, 1:18-cv-01810 (D. Del.). Pet. 60; Paper 5, 2.

The parties additionally identify two other *inter partes* review proceedings as related to the present proceeding: 1) IPR2020-00143; and 2) IPR2020-00144; both challenging U.S. Patent No. 8,145,879 B2, which claims priority to the application from which the '388 patent issued. Pet. 60; Paper 5, 2.

II. THE CLAIMED SUBJECT MATTER

A. The '388 Patent

The '388 patent is titled "Computer Memory Architecture for Hybrid Serial and Parallel Computing Systems." Ex. 1001, code (54). As background, the '388 patent describes that many applications require both serial and parallel processing, and a known drawback of such systems is that "[m]any parallel systems are engineered to perform tasks with high or massive parallelism, but are not sufficiently scaleable to effectively support limited parallelism in code, and in particular, do not efficiently process serial code." *Id.* at 1:29–35. To address this problem, the '388 patent describes "a computing system including a serial processor and a plurality of parallel

processors configured to switch between serial processing and parallel processing," which "provides seamless transitions between parallel and serial processing modes, while maintaining memory coherence and providing sufficient performance for streaming applications." *Id.* at 1:58–67.

The '388 patent describes an embodiment of system 100 that may switch from a serial processing mode to parallel processing mode, and vice versa. *Id*. at 5:46–48. System 100 includes: serial processor 14, serial memory 16, plurality of parallel processors 12, and plurality of partitioned memory modules 10. *Id*. at 4:30–33, Fig. 2. We reproduce Figure 2 below.

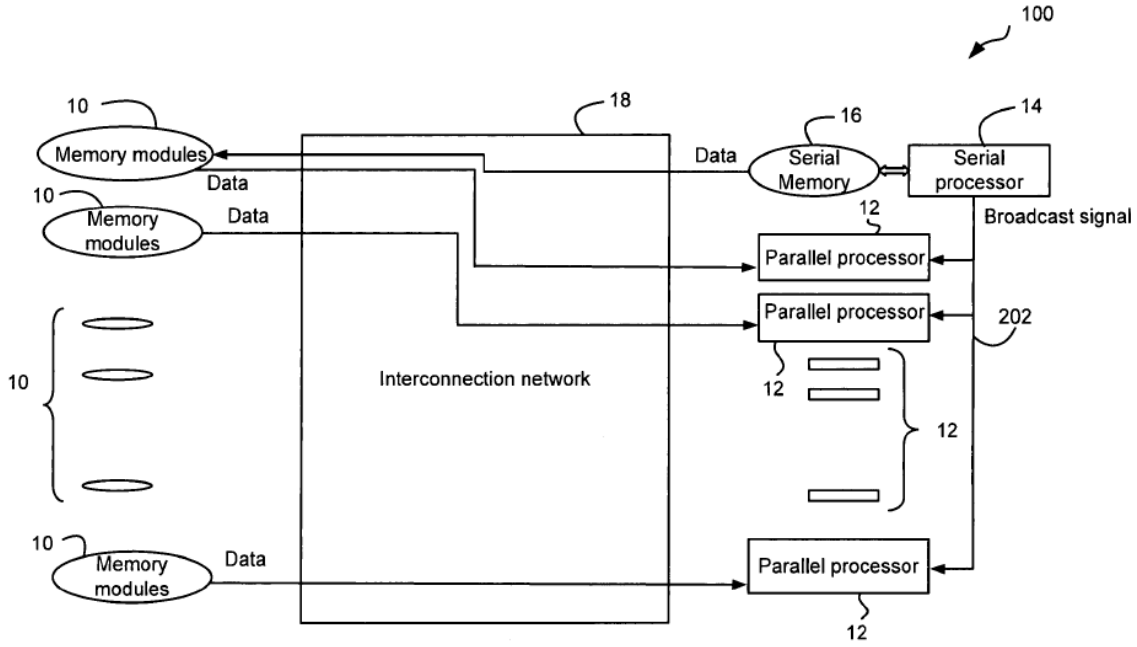

Fig. 2

> Figure 2, above, is a block diagram that illustrates a computing system embodiment that switches from serial processing mode to parallel processing mode. *Id.* at 3:63–65.

Figure 4, reproduced below, illustrates a command timeline for switching between processing modes.

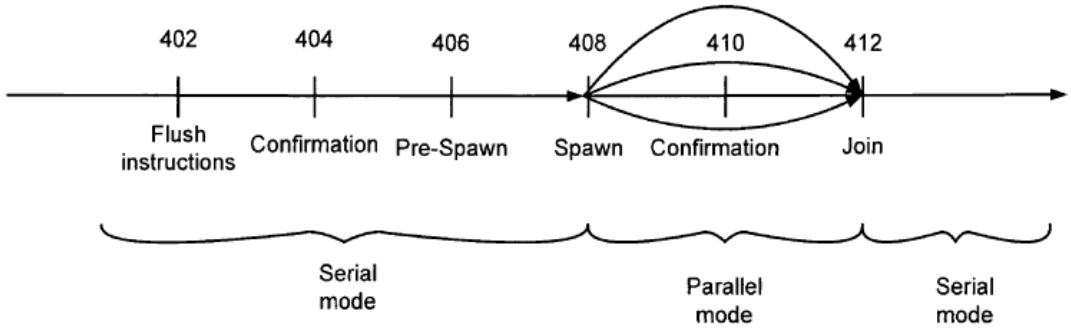

Fig. 4

> Figure 4, above, "is a diagram illustrating an example timeline and transitions between serial and parallel processing modes for a programming model for an example software program." *Id.* at 4:1–3.

Serial processor 14 of system 100 processes software instructions serially, and when desired, plurality of parallel processors 12 process the software instructions in parallel. *Id*. at 5:46–52.

In one embodiment, to switch from serial to parallel processing mode, serial processor 14 commands data flushing (step 402, flush instruction step). *Id.* at 2:12–16; 5:53–56; 9:17–21; Figs. 2, 4. Specifically, serial processor 14 provides for transfer of data from serial memory 16 to at least one of plurality of partitioned parallel memory modules 10 so that parallel processors 12 can access that data. *Id.* at 6:54–58.

Next, at least one of plurality of partitioned memory modules 10 acknowledges to serial processor 14 that the data has been queued (step 404). *Id*. at 2:26–33, 9:21–28, Figs. 2, 4. Subsequently, serial processor 14 broadcasts a "prefetching signal" to the parallel processors 12 to start prefetching data from the partitioned memory modules (pre-spawn step

406). *Id.* at 9:29–32; Figs. 2, 4. Serial processor 14 may then broadcast a command to change from serial processing mode to parallel processing mode (spawn step 408). *Id.* at 9:45–49, Fig. 4. After parallel processors 12 each receive acknowledgements confirming their data will be committed to memory modules 10 (step 410), computing system 100 may switch back to serial processing (step 412). *Id.* at 10:19–38, Fig. 4.

B. Claim 1

The '388 patent includes 39 claims, all of which are challenged here. Claims 1, 19, 32, and 33 are independent. *See* Ex. 1001, 13:51–18:3. Claim 1, which is representative, recites:

> 1. An apparatus comprising:
>
> a serial processor adapted to execute software instructions in a software program primarily in serial;
>
> a serial memory adapted to store data for use by the serial processor in executing the software instructions primarily in serial;
>
> a plurality of parallel processors adapted to execute software instructions in the software program primarily in parallel; and
>
> a plurality of partitioned memory modules adapted to store data for use by the plurality of parallel processors in executing the software instructions primarily in parallel;
>
> wherein the serial processor is further adapted, prior to a transition from a serial processing mode to a parallel processing mode, to provide for a transfer of updated data from the serial memory to at least one of the plurality of partitioned memory modules and to receive a corresponding acknowledgement from the at least one of the plurality of partitioned memory modules that the updated data has been queued or committed prior to any memory requests from the plurality of parallel processors.

Id. at 13:51–14:5.

C. Claim Construction[1]

1. "adapted to" – claims 1–32

Independent claims 1, 19, and 32 each recite that the serial processor is "adapted to" execute software instructions in a software program "primarily in serial," and similarly recite that the plurality of parallel processors are "adapted to" execute software instructions in the software program "primarily in parallel." Dependent claims 2–18 and 20–31 include these limitations by virtue of dependence from independent claims 1 and 19, respectively. Claims 33–39 do not contain these limitations.

The phrase "adapted to" has been understood to have both a broader meaning ("configured to"[2]) and a narrower meaning ("designed to"). *In re Giannelli*, 739 F.3d 1375, 1379 (Fed. Cir. 2014); *In re Man Machine Interface, LLC*, 822 F.3d 1282, 1286 (Fed. Cir. 2016). Patent Owner asserts that the narrower meaning applies to claims 1–32. Prelim. Resp. 24–26. In support, Patent Owner points to the following portion of the Specification.

> Serial processor 14 is configured to process a software program in serial. For example, software instructions in the software program may be executed serially as in a von Newmann or other sequential architecture or the like.
>
> Plurality of parallel processors 12 are configured to execute software instructions in a software program in parallel.

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[1] In this *inter partes* review based on a petition filed after November 13, 2018, the claim construction standard to be applied is the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b). The claim construction standard is that used by Article III federal courts, which follow *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc), and its progeny. *See* Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board, 83 Fed. Reg. 51,340, 51,344 (Oct. 11, 2018) (codified at 37 C.F.R. pt. 42 (2019)).

[2] Also referred to as "capable of," or "suitable for."

> . . . Parallel processors 14 may include thread control units (TCUs) that execute threads in parallel. . . . In general, the functionality of serial and parallel processors may be achieved in any suitable design including processors, custom or semi-custom circuitry, gate arrays, programmable logic arrays, etc.

Ex. 1001, 4:39–53 (cited at Prelim. Resp. 25). Patent Owner's expert, Professor Annavaram, opines that the serial and parallel processors of the '388 patent are disclosed as each having a specific design to carry out serial or parallel operation, respectively. Ex. 2001 ¶¶ 67, 68.

The disclosure Patent Owner cites expressly states that the serial and parallel processors are "configured to" process in serial or parallel, respectively. This supports the broader interpretation of "adapted to" as "configured to."

The Specification includes another disclosure that is even more on point. Specifically, the '388 patent describes an embodiment that includes a plurality of parallel processors coupled to the interconnection network and "*adapted (or, equivalently, configured) to* execute software instructions in the software program substantially in parallel." Ex. 1001, 2:59–3:6 (emphasis added). In other words, the Specification equates "adapted to" with the boarder meaning of "configured to." Significantly, this use of "adapted to" is with regard to the very limitation at issue (i.e., the respective processors being adapted/configured to execute software instructions primarily in serial or parallel).

Further, the term "adapted to" is also used in the dependent claims to mean "configured to." *See, e.g., Rexnord Corp. v. Laitram Corp.,* 274 F.3d 1336, 1342 (Fed. Cir. 2001) (a claim term should be construed consistently with its appearance in other claims of the same patent). For example, dependent claim 4 adds that the serial processor is further "adapted to"

broadcast a pre-fetch signal to the plurality of parallel processors. Ex. 1001, 14:14–19. The Specification discloses that the serial processor is "*adapted (or configured) to* send a signal to start pre-fetching of data from the shared memory. *Id*. at 3:34–39 (emphasis added). A person of ordinary skill in the art would understand that the '388 patent discloses that "adapted to" is equivalent to "configured to."

We preliminarily determine that "adapted to" as recited in claims 1–32 means "configured to."

2. Antecedent basis, claim 7

Claim 7 depends from claim 1 and recites "wherein the prefetched data is stored in a second memory in at least one of the plurality of processors." Independent claim 1 does not provide an antecedent basis for the phrase "the prefetched data.'" Petitioner asserts two possibilities: one, that claim 7 should recite "prefetched data" without the word "the," or two, that claim 7 was intended to depend from clam 4. *See* Pet. 42. Patent Owner does not address construction of this term.

We ask that the parties construe this term to the extent necessary to resolve this dispute.[3]

3. Other Claim Terms

Regarding other claim terms, Petitioner asserts that the ordinary and customary meaning should be applied. Pet. 11. Patent Owner does not address claim terms other than "adapted to" as addressed above. *See* Prelim. Resp. 24–26.

[3] An *inter partes* review cannot include a ground of indefiniteness under 35 U.S.C. § 112. *See* 35 U.S.C. § 311(b).

We determine that no other claim term requires express construction for purposes of this Decision. *See, e.g.*, *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) ("[W]e need only construe terms 'that are in controversy, and only to the extent necessary to resolve the controversy.'" (quoting *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999))).

4. Claim Construction is an Open Issue

Our claim interpretation here is preliminary and based on the record to this point. Claim construction remains an open issue in this proceeding, meaning that the parties may further address claim construction as needed to resolve this dispute.

III. PATENTABILITY

A. Asserted Grounds

Petitioner asserts that the challenged claims would have been unpatentable on the following grounds:[4]

[4] Petitioner supports its challenge with a Declaration by Dr. David Kaeli. (Ex. 1014), and Patent Owner relies on a Declaration by Dr. Murali Annavaram (Ex. 2001).

Claims Challenged	35 U.S.C. §	References
1, 3, 12–14, 17, 18	103(a)[5]	Nakaya, Nakamura, Koufaty[6]
2, 4–11, 15, 16, 19–39	103(a)	Nakaya, Nakamura, Koufaty, Vishkin[7]

B. Level of Skill in the Art

As explained below, we preliminarily accept Petitioner's view of the level of skill in the art. We also consider the prior art of record to be reflective of the level of skill in the art.

The parties differ somewhat with regard to the education and experience levels of a person of ordinary skill at the time of invention for the '388 patent.

Regarding education, the parties agree that a person of ordinary skill would have had a degree in the field of electrical and computer engineering or a related field. The parties disagree in that Petitioner contends that degree would be a Master's or Doctorate degree, while Patent Owner contends that it would be a Bachelor's degree. Pet. 8 (citing Ex. 1014 ¶¶ 33–36); Prelim. Resp. 22–24.

[5] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103. Because the challenged claims of the '388 patent have an effective filing date before the effective date of the relevant amendment, the pre-AIA version of § 103 applies.

[6] Ex. 1003, U.S. Pat. No. 5,978,830 (Nov. 2, 1999) ("Nakaya"); Ex. 1004, U.S. Pat. App. Pub. No. 2003/0177273 A1 (Sept. 18, 2003) ("Nakamura"); Ex. 1005, "Data Forwarding in Scalable Shared-Memory Multiprocessors," IEEE Transactions on Parallel and Distributed Systems, Vol. 7, No. 12 (Dec. 1996) ("Koufaty").

[7] Ex. 1006, "Explicit Multi-Threading (XMT) Bridging Models for Instruction Parallelism" (1998) ("Vishkin").

Patent Owner attacks Petitioner's position on education level by asserting that the opinion of Petitioner's expert is entitled to little or no weight because it lacks factual predicates. Prelim. Resp. 22 (citing 37 C.F.R. § 42.65(a)). Contrary to Patent Owner's contention, Dr. Kaeli's opinion is not wholly without factual predicates. For example, his opinion is based on his experience (Ex. 1014 ¶¶ 4, 6–14, App'x B), certain enumerated materials (Ex. 1014 ¶ 5), and legal standards (Ex. 1014 ¶¶ 15–16, 20–28, 33–35). Patent Owner does not contest any of these underlying bases.

Regarding experience, the parties agree that a person of ordinary skill would have about three years of experience. The parties differ in that Petitioner contends that the experience would be in parallel computing architectures, while Patent Owner more broadly contends the experience would be in computer architecture. Pet. 8 (citing Ex. 1014 ¶¶ 33–36); Prelim. Resp. 22–23 (citing Ex. 2001 ¶ 21).

In support of that contention, Patent Owner goes on to assert that Petitioner's proposed skill level is too high because many of Petitioner's references cite graduate students, who often do not have an advanced degree. Prelim. Resp. 22 (citing Dr. Annavaram's Declaration, Ex. 2001 ¶ 20). Specifically, Dr. Annavaram states that the Wen reference is a doctorate thesis, and both the Vishkin paper and Dr. Kaeli's declaration cite as background to research projects at various universities.[8] Ex. 2001 ¶ 20. Patent Owner adds, with supporting expert testimony, that parallel computing is "an extremely complicated concept," and "a single change in the design may cause a cascade of unpredictable consequences." Prelim.

[8] Patent Owner does not identify which Exhibit is "the Wen Reference."

Resp. 23–24 (citing Ex. 2001 ¶¶ 22–27). Based on these contentions, Patent Owner concludes that increased knowledge and insight is possessed by a person with above-average skill, not a person of ordinary skill in the art. *Id*. at 24 (citing Ex. 2001 ¶ 28).

We see no meaningful distinction between the parties' contentions on experience. In particular, Patent Owner's broader recitation of experience in "computer architecture" would include both serial and parallel processing. Additionally, Patent Owner's argument and evidence that parallel computing is complicated and that parallel computing design can have unpredictable consequences undermines rather than supports Patent Owner's contention that Petitioner's level of skill is too high.

The level of skill in the art remains an open issue in this proceeding, meaning that we have not made a final determination, and future submittals by the parties may include argument and evidence that would assist resolution of this proceeding. We provide the following guidance.

We note that the parties only address two aspects (education and experience) of the numerous aspects of the level of skill in the art. *See generally Daiichi Sankyo Co. v. Apotex, Inc*., 501 F.3d 1254, 1256 (Fed. Cir. 2007) (The following non-exhaustive list of factors can be relevant to a determination of the level of ordinary skill in the art: (1) educational level of the inventor; (2) type of problems encountered in the art: (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology, and (6) educational level of workers active in the field. Not all factors are present in every case, and one or more of these or other factors may predominate in a particular case). We also note that the level of skill in the art is only useful if tied to an obviousness analysis. *See generally Graham v. John Deere Co.*, 383 U.S. 1, 17–18

(1966); *Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (The "level of skill in the art is a prism or lens through which a judge, jury, or the Board views the prior art and the claimed invention."); *Ryko Mfg. Co. v. Nu-Star, Inc*., 950 F.2d 714, 718 (Fed. Cir. 1991) ("The importance of resolving the level of ordinary skill in the art lies in the necessity of maintaining objectivity in the obviousness inquiry.").

In light of this, we ask that if the parties provide additional argument and evidence related to the level of skill in the art, that argument and evidence should address any aspect of the level of skill in the art that influences the obviousness analysis, and that argument and evidence should explicitly address how that level impacts the obviousness analysis.

C. Secondary Considerations

Petitioner contends that none of the claims of the '388 patent were commercially successful, filled a long-felt need, or received industry praise. Pet. 59–60. Patent Owner does not present evidence of secondary considerations in the Preliminary Response.

We make no determination regarding secondary considerations at this time, and we do not factor secondary considerations into our obviousness analysis.

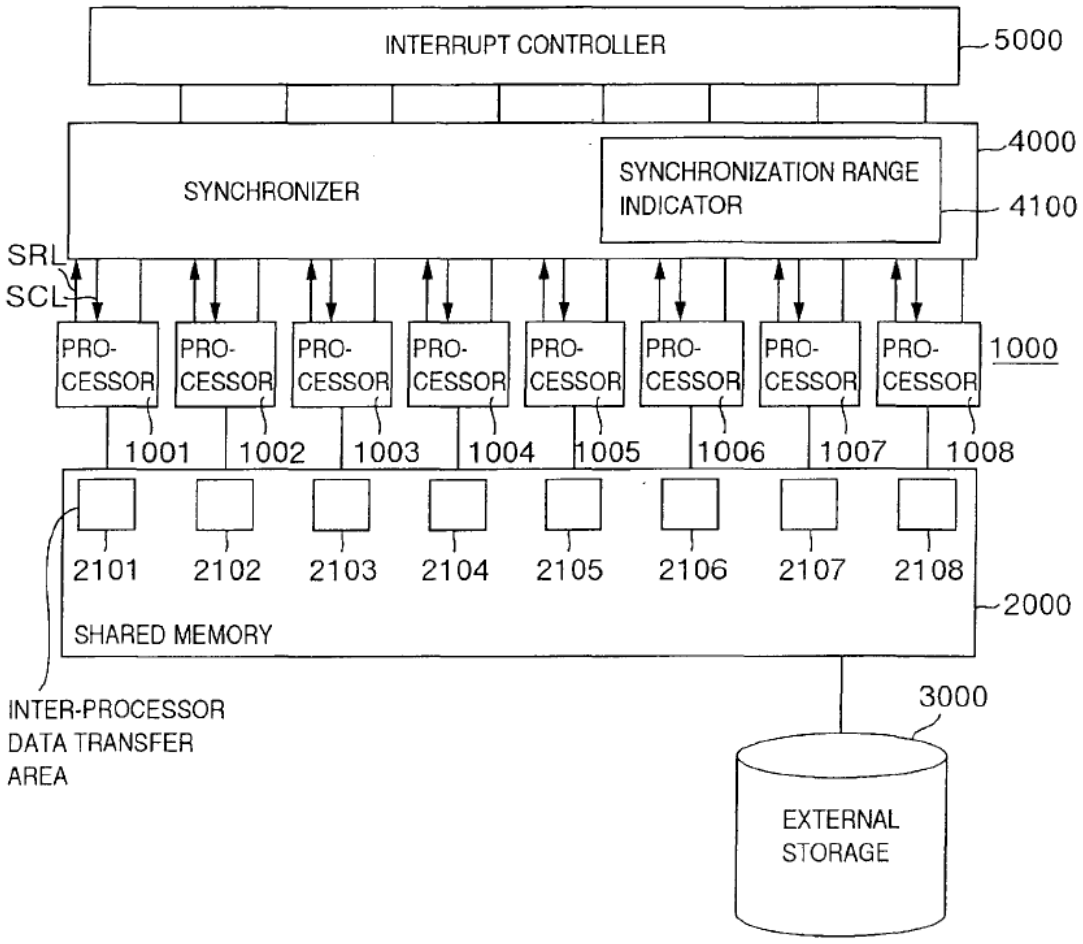
D. Obviousness over Nakaya, Nakamura, and Koufaty

Petitioner asserts that claims 1, 3, 12–14, 17, and 18 are unpatentable as obvious over Nakaya, Nakamura, and Koufaty. *See* Pet. 12–33. For the reasons expressed below, we determine that Petitioner has demonstrated a reasonable likelihood of establishing that claims 1, 3, 12–14, 17, and 18 are unpatentable as obvious.

1. Overview of Nakaya (Ex. 1003)

Nakaya is titled "Multiple Parallel-Job Scheduling Method and Apparatus," and relates to "a multiple parallel-job scheduling method and apparatus suitable for parallel or concurrent execution of a plurality of parallel information processing programs." Ex. 1003, code (54), 1:5–9. Specifically, Nakaya describes a computer system that includes a group of processors 1000 that are each connected to shared memory 2000 to read/write data. *Id.* at 7:60–64. For example, group of processors 1000 could include processors 1001–1004 that constitute or behave as serial processors and processors 1005–1008 that constitute or behave as parallel processors. *Id.* at 8:32–37. Synchronizer 4000 is connected to and executes synchronous control of processors 1001–1008. *Id.* at 8:55–58. Nakaya's Figure 1 follows.

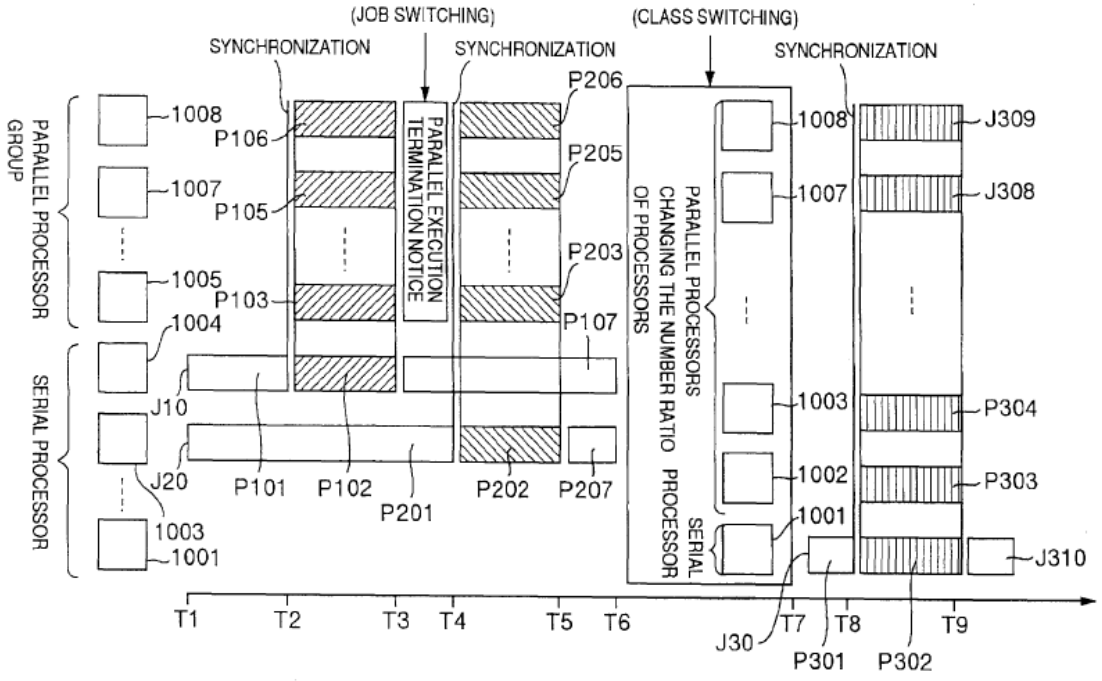
FIG.1



Nakaya's Figure 1, above, "is a diagram showing the overall construction of a computer system." *Id.* at 6:12–13.

Nakaya describes a method of assigning multiple processors to jobs and dynamically changing the number ratio of serial processors to parallel processors. *Id.* at 13:3–6; Fig. 8. Nakaya's Figure 8 follows.

FIG.8



Nakaya's Figure 8, above, is a diagram explaining the outline of multiple execution of parallel jobs. *Id.* at 6:32–33, 13:1–2.

For example, in an embodiment, during time interval T1 to T6, processors 1001 to 1004 behave as serial processors and processors 1005 to 1008 behave as parallel processors. *Id.* at 13:9–12. After time T6, only processor 1001 behaves as a serial processor, and processors 1002–1008 behave as parallel processors. *Id.* at 13:12–15.

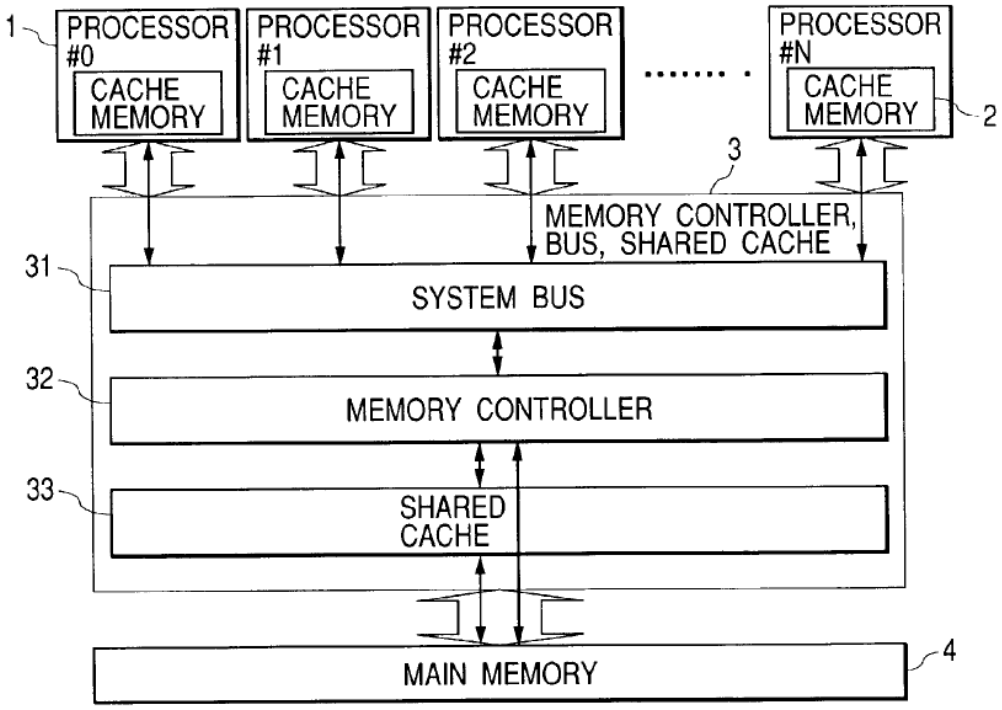
2. Overview of Nakamura (Ex. 1004)

Nakamura is titled "Data Communication Method in Shared Memory Multiprocessor System," and relates to "realizing data communication with coherence being maintained and speed-up of such data communication, and further to coherence control." Ex. 1004, code (54), ¶ 1. Nakamura discloses that "[i]n a shared memory multiprocessor system where a plurality of

processors share a memory, it is necessary to communicate shared data between the processors upon executing parallel programs." *Id.* ¶ 2.

In Nakamura's shared memory multiprocessor system, each processor has an allocated register for shared data communication and that data includes a duplicate of the other processors' registers. *Id.* ¶¶ 18–19. The processors communicate through ring type network communication channels. *Id.* ¶ 19. One of a plurality of processors is the main processor, and the other processors are subordinate. *Id.* ¶ 20. We reproduce Nakamura's Figure 1 below.

FIG. 1



Nakamura's Figure 1, above, is a diagram showing a configuration of a shared memory multiprocessor system. *Id.* ¶ 23.

As illustrated in Figure 1, Nakamura's shared memory multiprocessor system includes multiple processors 1, system bus 31, memory controller 32, and main memory 4. *Id.* ¶ 33. The system also includes a cache memory 2, and can include a shared cache 33. *Id.* ¶ 34.

3. Overview of Koufaty (Ex. 1005)

Koufaty is a printed publication titled "Data Forwarding in Scalable Shared-Memory Multiprocessors," and relates to the problem that "[s]calable shared-memory multiprocessors are often slowed down by long-latency memory accesses." Ex. 1005, Abstract. Koufaty discloses that data forwarding is a way to address this problem, such that "when a processor produces a datum, in addition to updating its cache, it sends a copy of the datum to the caches of the processors that the compiler identified as consumers of it." *Id.* This way, "when the consumer processors access the datum, they find it in their caches." *Id.* In other words, "when a processor updates a word in its cache, it also propagates the update to the caches of processors that are expected to use the word in the near future." *Id.* at 2.

4. Independent Claim 1

Claim 1 is the sole independent claim among this group of challenged claims. Ex. 1001, 13:51–15:4. Petitioner argues that the teachings of Nakaya, Nakamura, and Koufaty render claim 1 unpatentable as obvious. *See* Pet. 12–29.

a) Petitioner's Ground of Unpatentability

Petitioner contends that Nakaya describes a serial processor. Pet. 19–20 (citing Ex. 1003, Abstract, 8:12–19, 8:32–54, 13:7–16, 15:29–61, Figs. 1, 8; Ex. 1014 ¶¶ 102–107). Petitioner contends that Nakaya describes a plurality of parallel processors. Pet. 22–23 (citing Ex. 1003, Abstract, 8:12–25, 8:32–54, 13:7–16, 15:29–46, Fig. 8; Ex. 1014 ¶¶ 114–118). Petitioner

contends that Nakaya describes, or at least renders obvious, a plurality of partitioned memory modules. Pet. 23–25 (citing Ex. 1003, 7:63–8:7, 17:1–10, 17:40–46, 24:35–44, Figs. 1, 9; Ex. 1014 ¶¶ 119–124).

Petitioner recognizes that "Nakaya does not explicitly disclose local memories within its processors," but contends that Nakamura describes a serial memory. Pet. 13–14, 20–21 (citing Ex. 1004 ¶¶ 34, 37, Fig. 1; Ex. 1003, Figs. 1, 8; Ex. 1014 ¶¶ 108–113). Petitioner asserts that a person of ordinary skill in the art would have included Nakamura's cache memory in each of Nakaya's processors because they "would have operated more efficiently if each processor were provided with an additional local memory to increase the speed of processing data retrieved from the shared memory." Pet. 12–15 (citing Ex. 1004 ¶ 37, Fig. 1; Ex. 1003, Abstract, 7:63–8:7, 8:12–19, 8:32–54, Fig. 1; Ex. 1014 ¶¶ 83–88).

Petitioner acknowledges that Nakaya alone does not describe a serial processor adapted to provide for a transfer of updated data from the serial memory to at least one of the plurality of partitioned memory modules prior to a transition from a serial processing mode to a parallel processing mode (transfer of updated data), but Petitioner contends Koufaty combined with Nakaya discloses this element. *See* Pet. 26–27 (citing Ex. 1005, 1–3; Ex. 1003, 9:13–34, 17:1–10; Ex. 1014 ¶¶ 125–130). Specifically, Nakaya discloses a "synchronization" process to transition from serial to parallel processing, and as part of that process, the initial data to start subsequent parallel computing is transferred to the parallel processors. Pet. 15–16 (citing Nakaya, 17:39–45; Ex. 1014 ¶ 89). Petitioner contends that although Nakaya does not provide the specifics, the initial data needed for that parallel processing is transferred into the "inter-processor data transfer areas" which is a shared memory for data transfers among processors.

Pet. 16. According to Petitioner, a person of ordinary skill would have been aware of approaches for scheduling data transfers, such as data forwarding and data pre-fetching disclosed by Koufaty. Pet. 16 (citing Ex 1014 ¶¶ 89–90). Petitioner contends that Koufaty discloses forwarding updated data from producer processors to consumer processors. Pet. 26. Petitioner contends that Koufaty discloses moving data from producer processors to consumer processors, and Nakaya provides the mechanism for doing so. Pet. 26. In other words, Koufaty's concept of providing data to the processor that needs it, could be incorporated in Nakaya's system. The modified device would pass data from the serial memory of a serial processor to the inter-processor data transfer areas (corresponding to a plurality of partitioned memory modules adapted to store data for use by the plurality of parallel processors). Pet. 26–27 (citing Ex. 1014 ¶ 129). According to Petitioner, Koufaty envisions such a use. Pet. 27 (citing Ex. 1014 ¶130). Petitioner concludes that a person of ordinary skill in the art would have applied Koufaty's data forwarding technique to Nakaya as modified by Nakamura, because: it would increase speed and efficiency, reduce processor latency, and "[s]uch an approach provides data to the processor ahead of its next task, which would speed up processing for subsequent tasks." Pet. 15–19 (citing Ex. 1005, 1–2; Ex. 1003, 7:63–8:67, 12:26–36, 17:1–10, 17:28–46, 18:3–9, Fig. 10; Ex. 1014 ¶¶ 89–95).

Petitioner also recognizes that Nakaya does not describe receiving a corresponding acknowledgement from at least one of the plurality of partitioned memory modules that the updated data has been queued or committed prior to any memory requests from the plurality of parallel processors, but contends Koufaty combined with Nakaya discloses this

element. *See* Pet. 27–29 (citing Ex. 1005, 2; Ex. 1003, 7:63–8:7, 9:33–34, 18:1–9, Fig. 10; Ex. 1014 ¶¶ 131–136).

b) Patent Owner's Challenges and Evidence

Patent Owner makes several arguments against the ground of unpatentability for claim 1.

(1) "adapted to"

Patent Owner argues that Petitioner fails to explain why Nakaya's serial processor is "adapted to" execute software instructions primarily in serial as recited in claim 1, because Nakaya's "'serial' processors have the same generalist functionality as the parallel processors, even when they are labelled as 'serial' rather than 'parallel' processors." Prelim. Resp. 26–35. In other words, Patent Owner argues that because Nakaya's processors perform equally well to process in either serial or parallel, those processors were not designed to process primarily in serial or primarily in parallel. This argument is unpersuasive because, as explained in our claim construction above, it is not commensurate in scope with claim 1. The serial and parallel processors of claim 1 need not be "designed to" execute software instructions in serial or parallel, respectively. Rather, all that claim 1 requires is that the serial and parallel processors are configured to perform the recited function.

(2) Transfer of updated data

Claim 1 includes the limitation that the serial processor is adapted, prior to transition from serial to parallel processing mode, to provide for a transfer for updated data from the serial memory to at least one of the plurality of partitioned memory modules. Patent Owner makes several contentions in support of the argument that the Petition does not adequately address this limitation.

Patent Owner argues that neither Nakaya nor Koufaty describes data transfer from a serial processor to a parallel processor prior to transition from a serial to a parallel mode as claimed. Prelim. Resp. 37–42. Patent Owner contends that Nakaya discloses transfer of starting addresses of code rather than data. *Id*. at 37–38. According to Patent Owner, both Nakaya and a person of ordinary skill recognize that addresses of code are not data. *Id*. at 39. Patent Owner contends that Petitioner's contention that Nakaya discloses transfer of initial data for parallel processing (Pet. 15–16 (citing Nakaya 17:39–45) is silent with regard to when that data is transferred. *Id*. at 39–40. Patent Owner also contends that Koufaty does not disclose the timing of the transfer of the updated data. *Id*. at 41–42.

Patent Owner's argument is not persuasive at this stage of the proceeding for several reasons.

First, Patent Owner's argument is unpersuasive primarily because it is an individual attack on each reference and does not address the ground as articulated by Petitioner. Petitioner did not contend that either Nakaya or Koufaty individually discloses data transfer as claimed. Rather, as explained above, Petitioner contends that Koufaty's technique of moving data where it will be needed (data forwarding from producer processors to consumer processors) can be implemented within the structure of Nakaya's shared memory (inter-processor data transfer areas corresponding to partitioned memory modules as claimed). *See* Pet. 15–19, 26–27.

Second, portions of Patent Owner's arguments are inapposite. Nakaya's disclosure regarding transfer of starting addresses is not responsive to the ground of unpatentability because Petitioner did not rely upon that disclosure as corresponding to transfer of updated data as claimed. *See* Pet. 15–16 (asserting that Nakaya's disclosure of initial data needed for

parallel processing as the claimed updated data, and citing Nakaya, 17:39–45; Ex. 1014 ¶ 89). Likewise, Patent Owner's argument that Koufaty does not disclose the timing of transfer of the updated data is inapposite because Petitioner relies on Nakaya for the timing of the transfer. *See* Pet. 26.

Third, we agree with Patent Owner that Nakaya does not explicitly disclose when the initial data necessary to start the execution of the parallel computing is transferred; however, given that Nakaya discloses that the data is "necessary to start the execution of parallel processing," the disclosure implies that data is transferred prior to the start of parallel processing. *See* Ex. 1003, 17:39–45.

Patent Owner argues that a person of ordinary skill in the art would not have been motivated to transfer updated data from a serial processor before a transition from serial to parallel mode because the change would not speed up the overall process. Prelim. Resp. 42–47. Essentially, Petitioner contends the modified device would be faster (Pet. 15–19), and Patent Owner contends it is slower. Here, there is a genuine issue of a material fact, and at this point in the proceeding, we must view in the light most favorable to Petitioner. *See* 37 C.F.R. § 42.108(c).

As detailed in the description of the ground of unpatentability above, when discussing incorporating Koufaty's data forwarding technique into Nakaya's system, Petitioner mentions that Koufaty discloses a use like the proposed modification in that when the consumer processor (the processor that will use the data) was not known, the data was sent to shared memory. *See* Pet. 27; Ex. 1014 ¶ 130. Patent Owner argues that Koufaty's shared memory is accessible by all processors, while, in contrast, Nakaya's memory is tied to a specific processor. Prelim. Resp. 47. According to Patent Owner, a transfer to a common shared memory such as Koufaty's is not a

transfer to at least one of the plurality of partitioned memory modules as claimed. *Id*. at 47–48. In contrast, according to Patent Owner, Nakaya's system needs to know the consumer processor (the processor that will use the data) before transfer of the data. *Id*. at 48. Based on this, Patent Owner contends that Petitioner has not explained why Nakaya and Koufaty render this limitation obvious. Stated differently, Patent Owner asserts that Petitioner's reasoning that Koufaty discloses sending data to shared memory when the consuming processor (processor that needs the data) is not known, makes little sense given that Nakaya's system utilizes memory that is processor specific so that the consuming processor must be known before the transfer of updated data.

To the extent that Patent Owner is arguing that Koufaty's shared memory does not correspond to a plurality of partitioned memory modules as claimed, that argument is not persuasive. Petitioner relies on Nakaya for that limitation, not Koufaty.

Further, Patent Owner's argument that Koufaty having shared memory undermines Petitioner's rationale for the proposed combination is also unpersuasive. The proffered reason for combining Nakaya and Koufaty is to speed up processing for subsequent tasks. *See* Pet. 15–19. Petitioner mentions that Koufaty discloses transfer to shared memory rather than a consumer processor as evidence of the compatibility of combining Koufaty's technique with Nakaya, and not directly as a reason for doing so. *See* Pet. 27 (citing Ex. 1014 ¶130).

(3) Hindsight Bias

Patent Owner argues that Petitioner's proposed combination of Nakaya, Nakamura, and Koufaty fails to present a competent analysis on

how specific modifications would have affected the subject matter as a whole, and relies on hindsight bias. *See* Prelim. Resp. 50–53.

As an example, Patent Owner asserts that Petitioner does not explain why, once modified to include cache for each processor, the combined system would still utilize the inter-processor data transfer instead of transferring data directly between processors. *Id*. at 51–52.

Petitioner reasons, with support from its expert, that the addition of cache memory, as disclosed by Nakamura, to Nakaya's system would make the system operate more efficiently by increasing the speed of processing data retrieved from a memory dedicated to that processor. Pet. 12–15 (Ex. 1014 ¶¶ 83–88). A weakness of Patent Owner's argument is that it does not directly address Petitioner's reasoning, instead arguing that perhaps the device could operate differently.

As a second example, Patent Owner argues that Petitioner has not shown a reasonable expectation of success in combining Nakaya and Koufaty because Petitioner has not explained how the system easily identifies consumer processors at compile time. *Id*. at 52–53. In support, Patent Owner's expert opines that trial and error would be required to optimize the use of scheduler and compiler in a particular design. *See* Ex. 2001 ¶ 27 (cited at Prelim. Resp. 53).

A weakness of Patent Owner's argument is that, even if we accept it as true that some trial and error would be required, that does not mean that a modification lacks a reasonable expectation of success. A reasonable expectation of success does not require conclusive proof of efficacy. *See also Hoffman La Roche Inc. v. Apotex, Inc*., 748 F.3d 1326, 1331 (Fed. Cir. 2014) ("Conclusive proof of efficacy is not necessary to show obviousness. All that is required is a reasonable expectation of success."). Some level of

trial and error is a routine part of design. At this point in the proceeding, Patent Owner's argument is not persuasive.

Having pointed out those weaknesses, we want to be clear that we have not determined Patent Owner's argument is without merit. As stated above, for purposes of this Decision we must view genuine issues of material fact in the light most favorable to Petitioner. The factual premises of Patent Owner's argument that the proposed modification would alleviate the need for inter-processor data transfer or would have lacked a reasonable expectation of success given the difficultly in determining the mapping between processors at compile time are not fully developed at this point in the proceeding.

c) Conclusion for claim 1

Based on the present record, we determine that Petitioner has established a reasonable likelihood that it would prevail in showing that the subject matter of claim 1 would have been obvious over the combination of Nakaya, Nakamura, and Koufaty.

5. Claims 3, 12, 13, and 18

Petitioner contends that claims 3, 12, 13, and 18 would have been obvious over Nakaya, Nakamura, and Koufaty. Pet. 29–31, 33. Patent Owner argues that Petitioner's analysis of claims 3, 12, 13, and 18 ignores that the proposed combination alters Nakaya's processor to add local caches in light of Nakamura and Nakamura transfers data directly between processors. Prelim. Resp. 49–50 (citing Nakamura ¶¶ 65–68, Figs. 3–6; Ex. 1014 ¶¶ 71–74. With that preface, Patent Owner then repeats two of the arguments asserted against the ground of unpatentability against claim 1. These arguments are unpersuasive for the reasons given in the analysis of the ground of unpatentability against claim 1.

With regard to claim 18, Patent Owner additionally argues that Petitioner's analysis is inconsistent with that of claim 1. Prelim. Resp. 53–54. In particular, Patent Owner alleges that the ground of unpatentability for claim 1 modifies Nakaya to include cache memory as disclosed in Nakamura, but the ground for claim 18 does not include this modification. *Id.*

We understand Petitioner's ground of unpatentability against claim 1 to modify Nakaya to include cache memory, as disclosed by Nakamura, but not to add cache memory as partitioned memory modules to store data for use by the plurality of processors. *See* Pet. 20–21, 23–25. For that reason, the ground of unpatentability is not inconsistent as Patent Owner alleges.

Based on the present record, we determine that Petitioner has established a reasonable likelihood that it would prevail in showing that the subject matter of claims 3, 12, 13, and 18 would have been obvious over the combination of Nakaya, Nakamura, and Koufaty.

6. Claims 14 and 17

Petitioner contends that claims 14 and 17 would have been obvious over Nakaya, Nakamura, and Koufaty. Pet. 32–33. Patent Owner presents no additional argument for claims 14 and 17. *See generally* Prelim. Resp. We have reviewed Petitioner's arguments and evidence and determine that Petitioner has shown a reasonable likelihood of prevailing with regard to these claims. *See* Ex. 1014 ¶¶ 147–150; Nakaya 13:65–14:12, 18:1–9; Nakamura ¶¶ 34, 37.

E. Obviousness over Nakaya, Nakamura, Koufaty, and Vishkin

Petitioner asserts that claims 2, 4–11, 15, 16, and 19–39 are unpatentable as obvious over Nakaya, Nakamura, Koufaty, and Vishkin.

Pet. 33–59. For the reasons expressed below, we determine that Petitioner has demonstrated a reasonable likelihood of establishing that claims 2, 4–11, 15, 16, and 19–39 are unpatentable as obvious.

1. Vishkin (Ex. 1006)

Vishkin is titled "Explicit Multi-Threading (XMT) Bridging Models for Instruction Parallelism" and relates to "an extension to a standard instruction set which efficiently implements PRAM-style algorithms using explicitly multi-threaded instruction-level parallelism (ILP)." Ex. 1006, Abstract. Vishkin describes that "[a] current trend in processor design is to increasing ILP—the number of instructions whose executions overlap in time." *Id.* at 1. Accordingly, Vishkin presents "[a] new computational paradigm, Explicit Multi-Threading (XMT), which applies to the full spectrum from algorithms through architecture," where it is hoped that "a hardware investment of between 2 to 3 orders of magnitude . . . in ILP will generally return a speed-up, relative to the serial paradigm, which is an order of magnitude less than the investment." *Id.* at 5 (emphasis omitted).

In describing the XMT computational paradigm, Vishkin notes that "[a] Spawn command marks a transition from a serial state to a parallel state," where "[a] typical Spawn instruction initiates *n* threads." *Id.* at 2–3. Further, Vishkin states that, to avoid cache misses, "prefetching could begin prior to a branch or spawn instruction, that precedes the memory access." *Id.* at 8.

2. Petitioner's Ground of Unpatentability

Petitioner builds on the prior ground of unpatentability by adding Vishkin. Specifically, Petitioner contends that Nakaya increases processing speed by increasing parallelism, but does not provide detailed algorithms or commands. Pet. 34. Petitioner contends that Vishkin's "threading"

technique could improve Nakaya by further increasing parallelism. *Id*. at 34–35.

3. Patent Owner's Arguments

Patent Owner makes the following arguments applicable to the claims as enumerated below.

a) All Claims subject to this Ground

Patent Owner repeats the argument that Petitioner used the challenged claims as a road map. Prelim. Resp. 57–60. Patent Owner repeats the argument that a person of ordinary skill would not have combined Nakaya, Nakamura, and Koufaty. Prelim. Resp. 54. These arguments are unpersuasive for the reasons given above.

Patent Owner contends that claims 2, 4–11, 15, and 16 recite "prior to a transition from a serial processing mode to a parallel processing mode, transfer of updated data from the serial memory to at least one of the plurality of partitioned memory modules," and claims 32–39 contain a similar requirement. Patent Owner argues that Vishkin does not remedy the shortcoming regarding this limitation in the prior ground of unpatentability. Prelim. Resp. 55. This argument is unpersuasive for the reasons given above.

b) Claims 2, 4–11, 15, 16, and 19–32

Patent Owner repeats the argument against the first ground of unpatentability that the serial process must be "adapted to execute software instructions in a software program primarily in serial." Prelim. Resp. 54–55. This argument is unpersuasive for the reasons given above.

c) Claims 4 and 19–39

Claim 4 and 19–32 each requires that "the serial processor is further adapted. . . to broadcast a prefetch/prefetching signal to the plurality of

parallel processors to start prefetching of data from at least a portion of the plurality of partitioned memory modules." Claim 33 includes a similar requirement. Claims 34–39 include this requirement by virtue of dependence from claim 33.

Patent Owner argues that the Petition fails to present any evidence that prior art taught broadcasting prefetch signals by a data generating processor. Prelim. Resp. 56–57. In particular, Patent Owner emphasizes that "Petitioner has not pointed to *any single reference* that teaches a data generating processor" that broadcasts a prefetch/prefetching signal as claimed. *Id*. at 57 (emphasis added).

A weakness of Patent Owner's argument is that it overstates the case by saying Petitioner has failed to present "any" evidence. Petitioner presents some evidence. *See* Pet. 34–37, 39–40 (including citations to the prior art and Dr. Kaeli's Declaration). A second weakness is that Patent Owner is attacking the references individually, which is inapposite because Petitioner did not contend that any reference individually discloses broadcasting a signal as claimed. Rather, Petitioner contends that incorporating both Koufaty's prefetch instruction and Vishkin's spawn instruction into Nakaya's system would result in broadcasting a pre-fetch signal as claimed. *See id.* at 34–37, 39–40.

Patent Owner's factual assertions regarding how the references operate are relevant and worthy of further consideration. *See* Prelim. Resp. 56–57. At this stage in the proceeding, these assertions are not fully developed.

d) Claim 7

As mentioned in the claim construction section above, Petitioner provides two interpretations for claim 7. *See* Pet. 42. Petitioner asserts that

claim 7 would have been obvious over Nakaya, Nakamura, Koufaty, and Vishkin under both interpretations. *Id*. at 42–44.

Patent Owner argues that Petitioner's analysis of claim 7 is inconsistent with Petitioner's analysis of claim 18. Prelim. Resp. 60–61. In particular, Patent Owner points out that the ground of unpatentability against claim 7 includes a cache for the parallel processors while the ground against 18 does not. Prelim. Resp. 60–61.

Claim 18 does not depend from claim 7; rather, claims 7 and 18 each depend from independent claim 1. For that reason, the ground of unpatentability against claim 18 is not built upon the ground against claim 7. We see no inconsistency in Petitioner proposing a different ground against claim 7 than against claim 18.

4. Conclusion

Based on the present record, we determine that Petitioner has established a reasonable likelihood that it would prevail in showing that the subject matter of claims 2, 4–11, 15, 16, and 19–39 are unpatentable as obvious over Nakaya, Nakamura, Koufaty, and Vishkin.

IV. CONCLUSION

For the reasons expressed above, we determine that Petitioner has demonstrated a reasonable likelihood of showing that claims 1–39 of the '388 patent are unpatentable. We institute an *inter partes* review of all challenged claims of the '388 patent on all grounds alleged by Petitioner. For clarity, those grounds are listed below:

Claims	35 U.S.C. § 103
1, 3, 12–14, 17, 18	Nakaya, Nakamura, Koufaty
2, 4–11, 15, 16, 19–39	Nakaya, Nakamura, Koufaty, Vishkin

This Decision does not reflect a final determination on the patentability of any claim. The burden remains on Petitioner to prove unpatentability of each challenged claim. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

V. ORDER

In consideration of the foregoing, it is hereby:

ORDERED that, *inter partes* review of claims 1–39 of U.S. Patent No. 7,707,388 B2 is instituted on all grounds in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

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