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Paper 15
Entered: November 1, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.,
MICRON SEMICONDUCTOR PRODUCTS, INC., and
MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

IPR2022-00744
Patent 10,489,314 B2

Before JON M. JURGOVAN, DANIEL J. GALLIGAN, and NABEEL U. KHAN, *Administrative Patent Judges.*

KHAN, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

A. Background and Summary

Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC (collectively "Petitioner") filed a Petition (Paper 2, "Pet.") requesting an *inter partes* review of claims 1–3, 5, 6, 8–10, and 12–14 ("the challenged claims") of U.S. Patent No. 10,489,314 B2 (the '314 patent," Ex. 1001). Netlist, Inc. ("Patent Owner") timely filed a Preliminary Response (Paper 9, "Prelim. Resp."). With our authorization, Petitioner filed a Reply (Paper 11, "Reply") and Patent Owner filed a Sur-reply (Paper 12, "Sur-reply") addressing the appropriateness of discretionary denial under 35 U.S.C. § 314(a).

An *inter partes* review may not be instituted "unless . . . the information presented in the petition . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a) (2018). Having considered the arguments and evidence presented by Petitioner and Patent Owner, we determine that Petitioner has demonstrated a reasonable likelihood of prevailing for at least one of the challenged claims of the '314 patent, and we institute an *inter partes* review as to the challenged claims of the '314 patent on all the grounds of unpatentability set forth in the Petition.

B. Related Proceedings

The parties identify the following matter as related to this case: *Netlist, Inc. v. Micron Technology, Inc. et al.*, Case No. 1:22-cv-00136 (W.D. Tex). Pet. 82; Paper 3, 1. Petitioner also has concurrently filed a petition challenging different claims of the '314 patent in IPR2022-00745. Pet. 82.

C. The '314 Patent (Ex. 1001)

The '314 patent, titled "Memory Module With Data Buffering," relates to a memory system that controls timing of memory signals based on timing information. Ex. 1001, codes (54), (57). Figure 1, reproduced below, illustrates a memory module. *Id.* at 5:53–55.

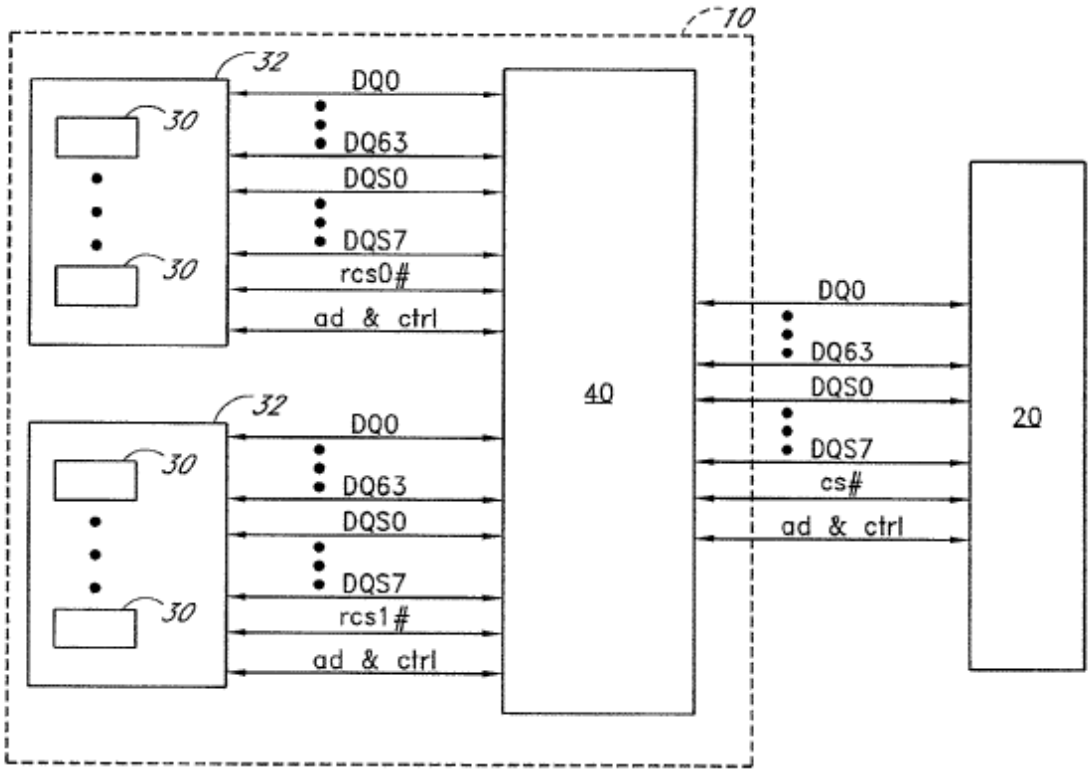


FIG. 1

As shown in Figure 1, memory module 10 is connectable to a memory controller 20 of a computer system (not shown). Ex. 1001, 5:53–56. The memory module 10 comprises a plurality of memory devices 30, each memory device having a corresponding load. *Id.* at 5:56–58. The memory module 10 further comprises a circuit 40 electrically coupled to the plurality of memory devices 30 and electrically coupled to the memory controller 20

of the computer system. *Id.* at 5:59–62. The circuit 40 selectively isolates one or more of the loads of the memory devices from the computer system. *Id.* at 5:62–64. The circuit 40 comprises logic that translates between a system memory domain of the computer system and a physical memory domain of the memory module 10. *Id.* at 5:64–67.

As described in the '314 patent, the plurality of memory devices 30 comprises a first number of memory devices 30, and the circuit 40 selectively isolates a second number of the memory devices 30 from the computer system, with the second number being less than the first number. Ex. 1001, 6:59–64. As also described in the '314 patent, the plurality of memory devices 30 are arranged in a first number of ranks, such as two ranks as illustrated in Figure 1. *Id.* at 6:65–7:1.

Figure 2, reproduced below, illustrates a circuit diagram of two memory devices of a memory module. Ex. 1001, 7:28–29.

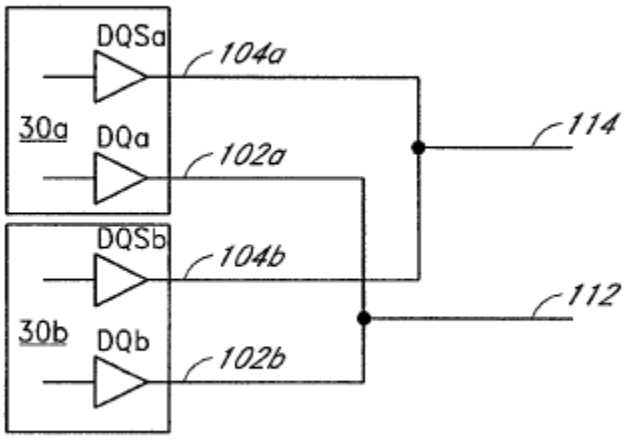


FIG. 2

As shown in Figure 2, the memory devices 30a, 30b have DQ data signal lines 102a, 102b and DQS data strobe signal lines 104a, 104b. Ex. 1001, 7:29–40. As further shown in Figure 2, the memory devices 30a, 30b have their DQ data signal lines 102a, 102b electrically coupled to a

common DQ line 112 and their DQS data strobe signal lines 104a, 104b electrically coupled to a common DQS line 114. *Id.* at 7:40–44. The common DQ line 112 and the common DQS line 114 are electrically coupled to the memory controller 20 of the computer system. *Id.* at 7:45–47.

As described in the '314 patent, the circuit 40 selectively isolates the loads of at least some of the memory devices 30 from the computer system. Ex. 1001, 7:49–51. In embodiments where the memory devices 30 are arranged in a plurality of ranks, the circuit 40 selectively isolates the loads of one, some, or all of the ranks of the memory module 10 from the computer system. *Id.* at 7:53–59.

D. Illustrative Claims

Claim 1, is the only independent claim of the '314 patent challenged in this Petition and is illustrative of the challenged claims. Claim 1 is reproduced below with limitation identifiers in brackets corresponding to claim analysis headings in the Petition. *See* Pet. 17–35.

> 1. [1a] A memory module operable in a computer system to communicate data with a memory controller of the computer system at a specified data rate via a N-bit wide data bus in response to memory commands received from the memory controller, [1b] the memory commands including a first memory command and a subsequent second memory command, the first memory command to cause the memory module to receive or output a first burst of N-bit wide data signals and a first burst of data strobes and the second memory command to cause the memory module to receive or output a second burst of N-bit wide data signals and a second burst of data strobes, the memory module comprising:
>
> [2] a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system;

> [3] a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks, [4a] wherein the plurality of N-bit wide ranks include a first rank configured to receive or output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command, [4b] and a second rank configured to receive or output the second burst of N-bit wide data signals and the second burst of data strobes at the specified data rate in response to the second memory command;
>
> [5] circuitry coupled between the plurality of N-bit wide ranks and the N-bit wide data bus; and
>
> [6] logic coupled to the circuitry and configured to respond to the first memory command by providing first control signals to the circuitry and to subsequently respond to the second memory command by providing second control signals to the circuitry, [7] wherein the circuitry is configured to enable data transfers through the circuitry in response to the first control signals and subsequently in response to the second control signals, [8] wherein respective N-bit wide data signals of the first burst of N-bit wide data signals and respective data strobes of the first burst of data strobes are transferred at the specified data rate between the first rank and the N-bit wide data bus through the circuitry, [9] and wherein respective N-bit wide data signals of the second burst of N-bit wide data signals and respective data strobes of the second burst of data strobes are transferred at the specified data rate between the second rank and the N-bit wide data bus through the circuitry;
>
> [10] wherein the data transfers through the circuitry are registered data transfers enabled in accordance with an overall CAS latency of the memory module, [11] and the circuitry is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry so that the overall CAS latency of the memory module is greater than an actual operational CAS latency of each of the plurality of memory integrated circuits.

Ex. 1001, 42:12–67.

E. Evidence

The Petition relies on the following references:

Reference	Exhibit No.
US 2002/0112119 A1; filed Mar. 13, 2002; published Aug. 15, 2002 ("Halbert").	1005
PC2100 and PC1600 DDR SDRAM Registered DIMM Design Specification, JEDEC Standard 21-C (January 2002) ("JESD21-C").	1006
DDR2 SDRAM Specification, JESD79-2A (January 2004) ("JESD79-2A")	1007

Petitioner also relies on the Declaration of Vojin G. Oklobdzija, Ph.D. (Ex. 1003) in support of its arguments. The parties rely on other exhibits as discussed below.

F. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–3, 5, 6, 8–10, and 12–14 would have been unpatentable on the following grounds:

Claim(s) Challenged	35 U.S.C. §	Reference(s)/Basis
1, 2, 6, 8, 12–14	103(a)[1]	Halbert
3, 9, 10	103(a)	Halbert, JESD21-C
5	103(a)	Halbert, JESD79-2A

Pet. 2–3.

[1] The Leahy-Smith America Invents Act ("AIA"), Pub. L. No. 112-29, 125 Stat. 284, 287–88 (2011), amended 35 U.S.C. § 103 and became effective March 16, 2013. Petitioner applies the pre-AIA version of § 103. Pet. 2–3.

II. ANALYSIS

A. Discretion under § 314(a)

As indicated above, Petitioner has concurrently filed with this Petition a parallel petition in IPR2022-00745. This Petition challenges claims 1–3, 5, 6, 8–10, and 12–14, while IPR2022-00745 challenges claims 15–20 and 22–33.

Patent Owner argues, *inter alia*, that we should exercise our discretion under 35 U.S.C. § 314(a) to deny institution because Petitioner has failed to sufficiently justify the two concurrently-filed petitions. Prelim. Resp. 16–22. Specifically, Patent Owner argues that the petitions are duplicative because both petitions use Halbert as the primary reference and a JEDEC standard as the secondary reference and that the parallel petitions place substantial and unnecessary burden on the Board and the Patent Owner. *Id*. at 19.

In its Reply, Petitioner argues that Patent Owner has asserted a large number of claims (29 total claims) against it in district court and that those claims are extremely lengthy requiring two petitions to address. Reply 1–2. Petitioner argues that it structured the petitions in a way to reduce prejudice to Patent Owner by asserting only a single ground for each asserted claim and having no overlapping claims between the petitions. *Id*. at 2. Petitioner distinguishes the two petitions by emphasizing that in IPR2022-00745 it challenges claims reciting a limitation that is not present in the claims in IPR2022-00744 except for in three dependent claims. *Id*. Petitioner does not, however, provide a ranking of the two petitions, arguing that because there is no claim overlap between the petitions and only a single obviousness ground per claim was proffered, it is not feasible for Petitioner to provide such a ranking. *Id*. at 5.

In the Sur-reply Patent Owner argues that Petitioner has not explained the differences between the petitions and has not provided a ranking, both of which are required by the PTAB Consolidated Trial Practice Guide (Nov. 2019) (available at https://www.uspto.gov/TrialPracticeGuideConsolidated) ("TPG"), and that Petitioner's refusal to comply with the TPG is indefensible. Sur-reply 1.

Upon consideration of the specific circumstances under which Petitioner filed two petitions, we decline to exercise our discretion to deny institution in this proceeding. We agree with Petitioner that a large number of claims have been asserted against it in district court and that addressing those 29 claims may necessitate filing two separate petitions. *See* TPG at 59 ("[T]he Board recognizes that there may be circumstances in which more than one petition may be necessary, including, for example, when the patent owner has asserted a large number of claims in litigation.") The fact that the same claims are not challenged between the two petitions weighs in favor of declining to exercise our discretion to deny institution. *See Gen. Plastic Co., Ltd. v. Canon Kabushiki Kaisha*, IPR2016-01357, Paper 19 at 16–17 (PTAB Sept. 6, 2017) (precedential as to § II.B.4.i).

We disagree with Patent Owner that Petitioner has not explained the differences between the two petitions. In its Reply, Petitioner explains that the two Petitions challenge different claims; that the independent claims challenged in IPR2022-00745 include a limitation that is not present in the independent claim challenged in IPR2022-00744; and that the prior art combinations relied upon are, at least partly, different between the two petitions.

Although the TPG advises that a "petitioner should, in its petitions or in a separate paper filed with the petitions, identify: (1) a ranking of the

petitions in the order in which it wishes the Board to consider the merits, if the Board uses its discretion to institute any of the petitions" (TPG at 59–60), we determine that Petitioner's failure to rank its petitions does not outweigh the other facts discussed above. We therefore decline to exercise our discretion under § 314(a) to deny institution based on the concurrently filed petitions.

B. Principles of Law

Petitioner bears the burden of persuasion to prove unpatentability of the claims challenged in the Petition, and that burden never shifts to Patent Owner. *Dynamic Drinkware, LLC v. Nat'l Graphics, Inc.*, 800 F.3d 1375, 1378 (Fed. Cir. 2015).

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) any objective evidence of obviousness or non-obviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

C. Level of Ordinary Skill in the Art

In determining the level of ordinary skill in the art, various factors may be considered, including the "type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field." *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995).

Petitioner contends a person of ordinary skill in the art "would have been someone with an advanced degree in electrical or computer engineering and at least two years of work experience in the field, or a bachelor's degree in such engineering disciplines and at least three years of work experience in the field." Pet. 3 (citing Ex. 1003 ¶ 52). Patent Owner asserts it "does not contest Petitioner's proffered definition of the level of a person of ordinary skill in the art." Prelim. Resp. 6.

For purposes of this Decision, we adopt Petitioner's proposed level of ordinary skill, except that we find that the phrase "at least" in Petitioner's proposed definition creates a vague, open-ended upper bound for the level of ordinary skill, and we therefore do not adopt that aspect of the proposal. Thus, we determine at this stage of the proceeding, that a person of ordinary skill in the art would have been a person with an advanced degree in electrical or computer engineering and two years of work experience in the field of memory module design and operation, or a bachelor's degree in such engineering disciplines and three years of work experience in the field.

D. Claim Construction

We apply the same claim construction standard used in district court actions under 35 U.S.C. § 282(b), namely that articulated in *Phillips v. AWH Corp.*, 415 F.3d 1303 (Fed. Cir. 2005) (en banc). *See* 37 C.F.R. § 42.100(b) (2020).

In applying that standard, claim terms generally are given their ordinary and customary meaning as would have been understood by a person of ordinary skill in the art at the time of the invention and in the context of the entire patent disclosure. *Phillips*, 415 F.3d at 1312–13. "In determining the meaning of the disputed claim limitation, we look principally to the intrinsic evidence of record, examining the claim language itself, the written

description, and the prosecution history, if in evidence." *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 469 F.3d 1005, 1014 (Fed. Cir. 2006) (citing *Phillips*, 415 F.3d at 1312–17).

Neither party propose any constructions for any claim terms. *See* Prelim. Resp. 9–10; *see also* Pet. 6–7.[2] We determine no terms need to be construed to resolve the disputes between the parties at this stage of the proceeding.

E. Obviousness over Halbert (Ground 1)

Petitioner argues claims 1, 2, 6, 8, and 12–14 of the '314 patent would have been obvious over Halbert. Pet. 17–44. Below we provide a brief overview of the prior art references and then analyze Petitioner's contentions in light of Patent Owner's arguments.

1. Halbert (Ex. 1005)

Halbert relates to memory module architectures and methods for operating digital memory devices and systems. Ex. 1005 ¶ 2. Figure 4, reproduced below, is a block diagram of a memory module. *Id.* ¶ 15.

[2] Petitioner indicates that "[t]he parties' proposed constructions from [the related litigations] are set forth in Exs. 1008–1009" but that "[t]he parties' construction disputes from the related litigations do not affect the outcome of this Petition with respect to any claim." Pet. 6–7.

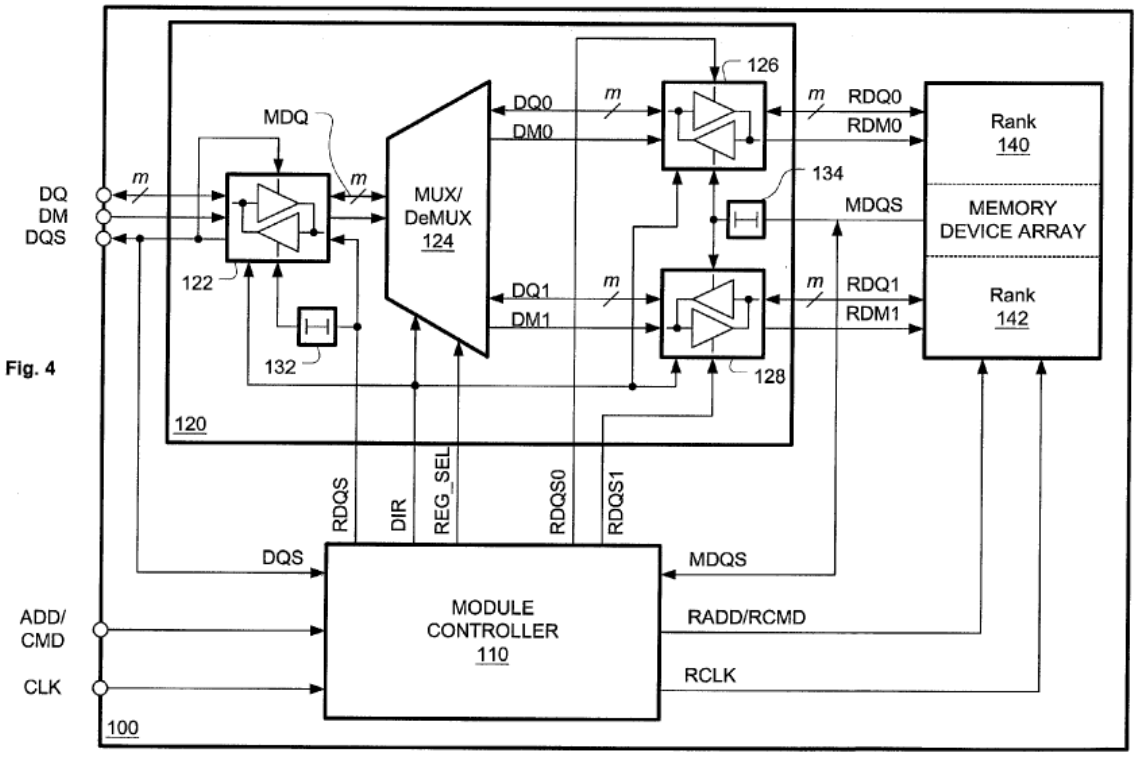
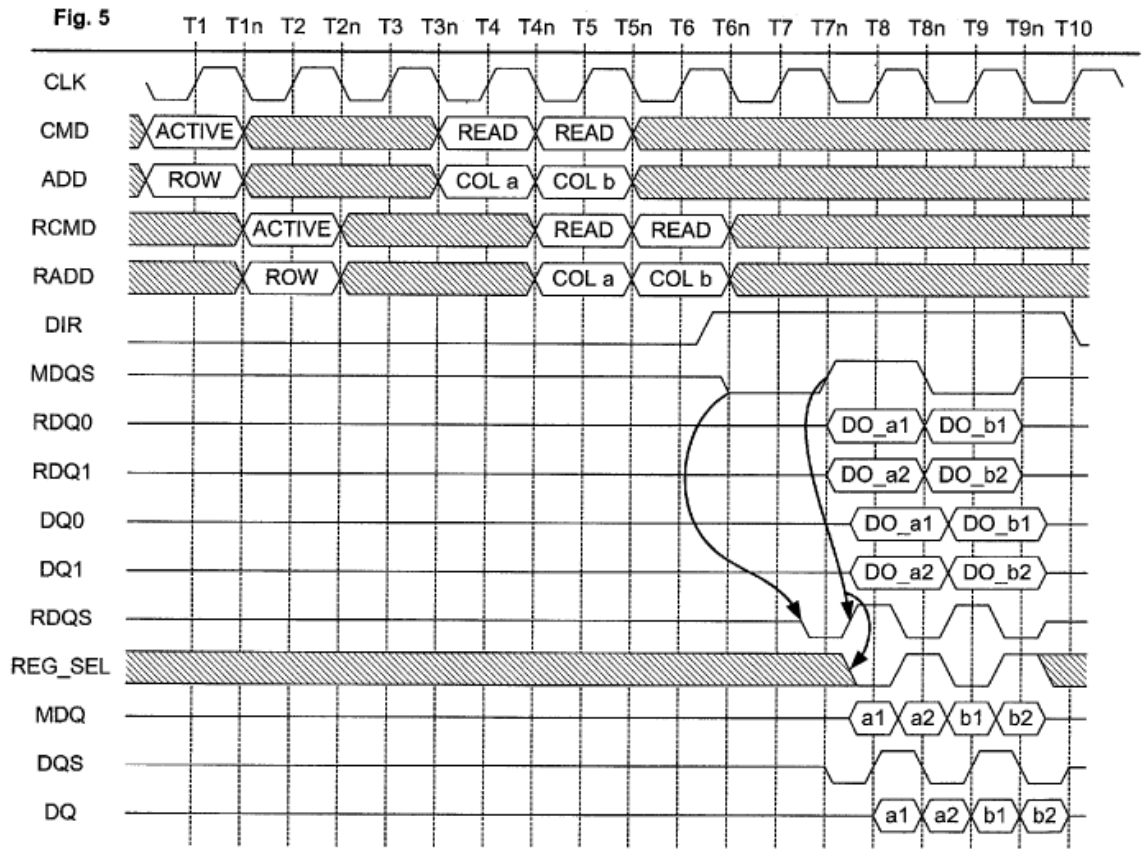


Fig. 4

As shown in Figure 4, memory module 100 includes three functional blocks: a module controller 110; a data interface circuit 120; and a memory device array 140/142. Ex. 1005 ¶ 28. The module controller 110 synchronizes the operation of module 100 with the attached memory system. *Id.* ¶ 29. Additionally, module controller 110 provides timing and synchronization signals to data interface circuit 120. *Id.* In Figure 4, a bi-directional buffer 122 is coupled to a bi-directional module data port that can be connected to a system memory data bus. *Id.* ¶ 31. Further, a data strobe signal DQS can be driven by buffer 122 onto the memory data bus. *Id.* Figure 5, reproduced below, shows a timing diagram for two consecutive read operations for the memory module of Figure 4. *Id.* ¶ 16.



Externally, a primary memory controller initiates READ operations. Ex. 1005 ¶ 37. As part of the READ operation, device array 140/142 signals that it is about to drive data onto buses RDQ0 and RDQ1 by taking data strobe MDQS low at T6n. *Id.* ¶ 38. At T7n, device array 140/142 takes MDQS high, signifying that data outputs "DO_a1" and "DO_a2" are being driven respectively onto buses RDQ0 and RDQ1. *Id.* ¶ 39. Delay element 134 delays MDQS long enough for the buses to settle, and then passes the MDQS strobe to registers 126 and 128. *Id.* Upon receiving MDQS, registers 126 and 128 latch DO_a1 and DO_a2. *Id.* Figure 8, reproduced below, shows a side view of multiple DIMM modules connected to a multi-drop memory bus. *Id.* ¶ 18.

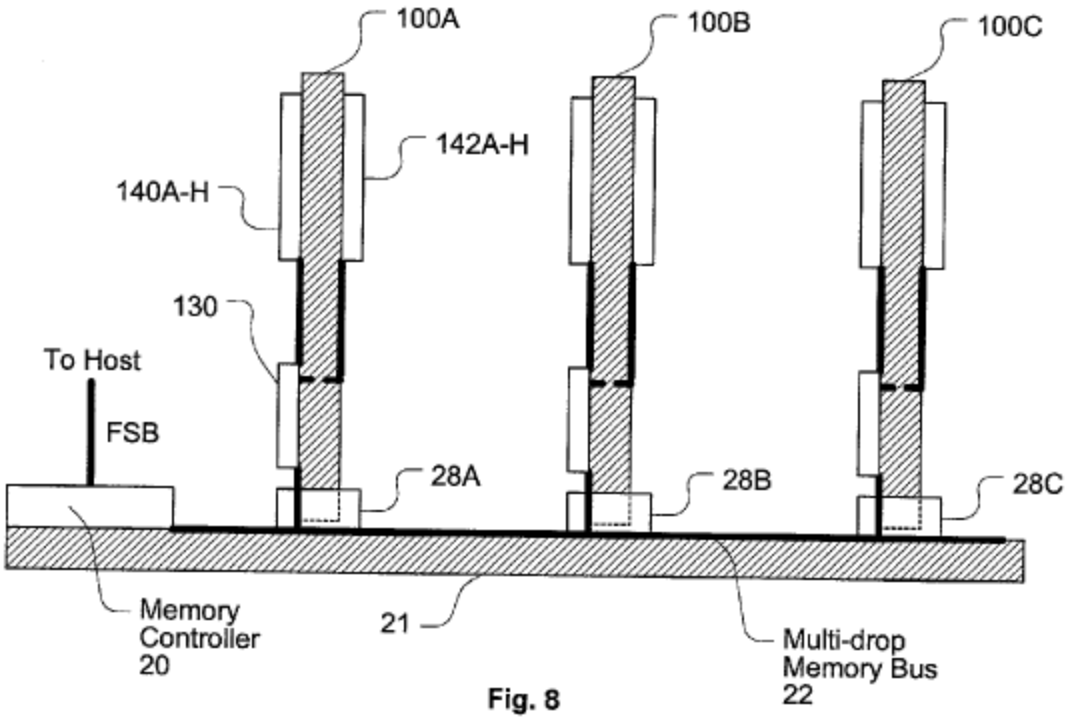


Fig. 8

Memory modules 100A, 100B, and 100C are arranged in a memory system with a primary memory controller 20 and a multi-drop memory bus 22. Ex. 1005 ¶ 49. With multiple modules, each module recognizes ACTIVE commands addressed to that module and respond accordingly. *Id.*

2. Analysis of Claim 1

Regarding limitation 1.1a, Petitioner argues that Halbert's memory module 100 teaches the recited "memory module," that Halbert's memory controller 20 teaches the recited "memory controller," and that memory bus 22 teaches the recited "data bus." Pet. 17–18. Petitioner argues that memory module 100 has a data interface 120 that provides for m-bit wide data transfers between the module and the system memory data bus. *Id*. at 18 (citing Ex. 1005 ¶¶ 5, 30, 49, Figs. 4, 8; Ex. 1003 ¶¶ 93–94). Petitioner further argues that Halbert's memory module enables data transfers at a "specified data rate" and that this data rate is twice the data rate of the

registered dual-bank DIMM. *Id*. at 18–19 (citing Ex. 1005 ¶ 24; Ex. 1003 ¶ 95).

Regarding limitation 1.1b, Petitioner argues that memory module 100 outputs and receives first and second bursts of m-bit-wide data signals (i.e. the recited N-bit wide data signals) and data strobes caused by first and second memory commands. Pet. 19 (citing Ex. 1005 ¶¶ 31, 37, Fig. 4; Ex. 1003 ¶ 96). These memory commands can be a read command and a subsequent write command or, in the alternative, can be a read command and a subsequent read command. *Id*. at 19–20 (citing Ex. 1005 ¶¶ 33, 35, 36–38, 41; Ex. 1003 ¶¶ 97–100).

Regarding limitation 1.2, Petitioner argues Halbert teaches a printed circuit board having a plurality of edge connections configured to be electrically coupled to a corresponding plurality of contacts of a module slot of the computer system. Pet. 21–22 (citing Ex. 1005 ¶¶ 6–7, cl. 11, Fig. 8; Ex. 1003 ¶¶ 102–104).

Regarding limitation 1.3, Petitioner argues Halbert teaches a plurality of memory integrated circuits mounted on the printed circuit board and arranged in a plurality of N-bit wide ranks. Pet. 22 (citing Ex. 1005 ¶¶ 27–28, 30; Fig. 4; Ex. 1003 ¶ 106).

Limitations 1.4a and 1.4b require first and second ranks configured to receive or output bursts of N-bit wide data signals and data strobes at the specified data rate in response to the first and second memory commands, respectively. Petitioner identifies Halbert's memory device ranks 140 and 142 as the respective first and second ranks and argues that they are configured to output the first and second bursts of N-bit wide data signals and strobes at the specified data rate in response to memory commands (a read command and subsequent write command or a read command and

subsequent read command). Pet. 22–24 (citing Ex. 1005 ¶¶ 33, 35, 37–38, Fig. 5; Ex. 1003 ¶¶ 108–109).

Regarding limitation 1.5, Petitioner identifies Halbert's data interface circuit 120 as the recited "circuitry coupled between the plurality of N-bit wide ranks and the N-bit wide data bus." Pet. 26 (citing Ex. 1005 ¶ 30, Fig. 4; Ex. 1003 ¶ 116).

Regarding limitation 1.6, Petitioner identifies Halbert's module controller 110 and control signals AWAY, TO, and REG_SEL as the recited "logic coupled to the circuitry and configured to respond to the first memory command by providing first control signals to the circuitry and to subsequently respond to the second memory command by providing second control signals to the circuitry." Pet. 27–28 (citing Ex. 1005 ¶¶ 34–35, Ex. 1005 ¶ 118–119).

Regarding limitation 1.7, Petitioner argues that in response to the first control signals, in AWAY mode, data transfers are enabled away from memory device ranks 140/142, through data interface 120 and buffer 122 toward system memory data bus. Pet. 28 (citing Ex. 1005 ¶¶ 35; Ex. 1003 ¶¶ 120–122).

Regarding limitations 1.8 and 1.9, Petitioner argues that Halbert's DIMM can provide twice the data rate of the dual-bank registered DIMM and that this is the claimed "specified data rate." Pet. 29 (citing Ex. 1005 ¶¶ 24, 35). Thus, according to Petitioner, a person of ordinary skill "would have understood that Halbert's memory module 100 enables data signals and strobes transfer from the memory device array *to the system memory data bus in response to read commands*, and from the system memory data bus *to the memory device array in response to write commands*, at the specified data rate, i.e., at twice the data rate of the registered DIMM." *Id*. (citing

Ex. 1005 ¶ 35; Ex. 1003 ¶¶ 123, 125, 127). Petitioner argues that Figure 4 of Halbert shows that the burst of data signals and strobes are transferred through the data interface circuit 120. Pet. 29–30.

Regarding limitation 1.10, Petitioner argues that Halbert discloses registers 126, 128, and 122 for providing registered data transfers through data interface 120. Pet. 30 (citing Ex. 1005 ¶ 36; Ex. 1003 ¶ 129). Further, Petitioner argues that the registered data transfers are enabled by module controller 110 in accordance with an overall CAS latency of memory module 100. *Id*. at 31 (citing Ex. 1005 ¶ 29, Fig. 5; Ex. 1003 ¶¶ 130–131).

Regarding limitation 1.11, Petitioner argues data interface circuit 120 is configured to add a predetermined amount of time delay for each registered data transfer through the circuitry because registers 126 and 128 add a predetermined time delay of one clock cycle for each registered data transfer through circuit 120. Pet. 33–34 (citing Ex. 1005, Fig. 5; Ex. 1003 ¶¶ 132–133). Petitioner argues that as a result, the overall CAS latency of memory module 100, e.g., from T4 to T8, is greater than the actual operational CAS latency of each of the plurality of memory integrated circuits, e.g., from T5 to T7n. *Id*. at 34–35 (citing Ex. 1005, Fig. 5; Ex. 1003 ¶¶ 132–133).

Patent Owner argues that claim 1 requires: (1) that the same specified data rate is used when transferring information between the memory module and memory controller as well as within the memory module (Prelim. Resp. 23); (2) that "the ***same*** first burst of data signals and data strobes are transferred between the module and the memory controller of the computer, and to or from the first rank within the memory module" (*id*. at 29–31); and (3) that the same first memory command causes the memory module and the first rank to receive or output the first bursts of data signals and strobes (i*d*.

at 31–32). Patent Owner argues that Petitioner has not shown that any of the three requirements above are taught by Halbert.

For example, Patent Owner argues that Figure 5 of Halbert shows instead that Halbert uses a different data rate between the memory module and the computer system than the data rate between memory ranks 140, 142 and data interface 120. *Id*. at 24–27 (citing Ex. 1005 ¶¶ 13, 24, 42, Figs. 4, 5). Similarly, Patent Owner argues that Figure 5 of Halbert shows that the first burst of data signals between the module and memory controller and to or from the first rank within the memory module are different. *Id*. at 29–31. And again, Patent Owner argues that in Halbert the memory command for the module causes two pieces of data to be received or output by the module, but the memory command presented to the ranks requests a single column of data and that, therefore, different memory commands are presented to the memory module versus the first and second ranks. *Id*. at 32–33.

Patent Owner further argues that claim 1 requires the first memory command to cause a burst of data to be received or output by the first rank and that a "burst" of signals requires at least two or more data signals. Prelim. Resp. 27–28 (citing Ex. 1001, 13:30–31, 13:35–37, 13:42–46, Figs. 6A, 6B, 7). Figure 5 of Halbert, according to Patent Owner, shows only one piece of data being transferred for rank 0 in response to the first read command. *Id*. at 28.

At this stage of the proceeding we are persuaded by Petitioner's arguments of a reasonable likelihood that Halbert teaches the limitations of claim 1 for the reasons summarized above. Petitioner supports its contentions with citations from Halbert and with unrebutted testimony from Dr. Oklobdzija. In relation to Patent Owner's arguments regarding the specified data rate specifically, Dr. Oklobdzija testifies that "Halbert

discloses that memory device rank 140 can be a first rank that is configured to output the first burst of N-bit wide data signals and the first burst of data strobes at the specified data rate in response to the first memory command." Ex. 1003 ¶ 107 (citing Ex. 1005 ¶¶ 33, 38). Dr. Oklobdzija also testifies that "[d]ata signals DQ0 are output to the memory data bus at the specified data rate" and that the "[m]emory device array 140 also outputs the first burst of data strobes at the specified data rate, i.e., memory data strobe MDQS, as part of the read operation." *Id*. ¶ 108 (citing Ex. 1005 ¶¶ 35, 37). Dr. Oklobdzija provides similar testimony for the second rank as well. *Id*. ¶¶ 109–114. Finally, Dr. Oklobdzija testifies that a person of ordinary skill "would have understood that Halbert's memory module 100 enables data and data strobes transfer from the memory device array to the system memory data bus in response to the read command at the specified data rate of twice the data rate of the registered DIMM." *Id*. ¶ 123.

Further in relation to arguments regarding the "burst" of signals, Dr. Oklobdzija testifies that "Halbert discloses that the memory module 100 receives and outputs bursts of N-bit wide data signals and data strobes. Ex. 1003 ¶ 96 (citing Ex. 1005 ¶¶ 31, 32). Based on the evidence presented at this stage of the proceeding we are not persuaded that the term "burst" recited in claim 1 should be limited to refer to at least two or more data signals. The citations Patent Owner relies upon from the '314 patent do not expressly limit the term in this manner (*see* Ex. 1001, 13:30–31, 13:35–37, 13:42–46) and Patent Owner does not present any other intrinsic or extrinsic evidence to support this construction. To the extent Patent Owner's argument focuses on the recitation of the plural term "signals," as explained above, Dr. Oklobdzija testifies that Halbert outputs "bursts of N-bit wide data signals." Ex. 1003 ¶ 96 (citing Ex. 1005 ¶¶ 31, 32).

Although we determine that Petitioner's contentions are sufficient at this stage of the proceeding, we note that Patent Owner's arguments raise several issues that would benefit from further development as trial progresses including what specifically claim 1 requires regarding the "specified data rate" and "burst" of signals limitations and whether Halbert teaches these limitations when properly construed. For example, the parties may wish to address whether claim 1 requires the same specified data rate to be used when communicating data between the memory controller of the computer system and the memory module over the N-bit wide data bus, as well as between the first and second ranks and the recited circuitry. Additionally, the parties may wish to provide further evidence and analysis (to the extent permitted by our rules) regarding the data rates used in Halbert between the data interface 120 and the computer system, the data rate between memory ranks 140, 142 and data interface 120, and the data rates through data interface 120.

3. Analysis of Claims 2, 6, 8, 12–14

Based on a review of the current record at this stage of the proceeding, Petitioner has made a sufficient showing of a reasonable likelihood that claims 2, 6, 8, 12–14 would have been obvious over Halbert. *See* Pet. 35–44. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See* Prelim. Resp.

4. Conclusion – Obviousness over Halbert (Ground 1)

Accordingly, having considered the arguments and evidence, we are persuaded that Petitioner has demonstrated a reasonable likelihood of prevailing on its challenge to claims 1, 2, 6, 8, and 12–14 of the '314 patent as obvious over Halbert.

F. Obviousness over Halbert and JESD21-C (Ground 2); Obviousness over Halbert and JESD79-2A (Ground 3)

Petitioner argues claims 3, 9, and 10 of the '314 patent would have been obvious over Halbert and JESD21-C (Pet. 45–66) and claim 5 would have been obvious over Halbert and JESD79-2A (Pet. 66–76). Based on a review of the current record at this stage of the proceeding, Petitioner has made a sufficient showing of a reasonable likelihood that the challenged claims under the aforementioned grounds would have obvious over the respective references. Patent Owner has not provided a separate response to these arguments at this stage of the proceeding. *See* Prelim. Resp.

III. CONCLUSION

Petitioner has demonstrated a reasonable likelihood of prevailing in showing the unpatentability of at least one challenged claim of the '314 patent. At this stage of the proceeding, however, we have not made a final determination with respect to the patentability of the challenged claims.

IV. ORDER

For the foregoing reasons, it is:

ORDERED that, pursuant to 35 U.S.C. § 314(a), an *inter partes* review of claims 1–3, 5, 6, 8–10, and 12–14 of the '314 patent is instituted with respect to all grounds of unpatentability set forth in the Petition; and

FURTHER ORDERED that, pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4(b), *inter partes* review of the '314 patent shall commence on the entry date of this Order, and notice is hereby given of the institution of a trial.

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